

100V N-Channel Split Gate MOSFET

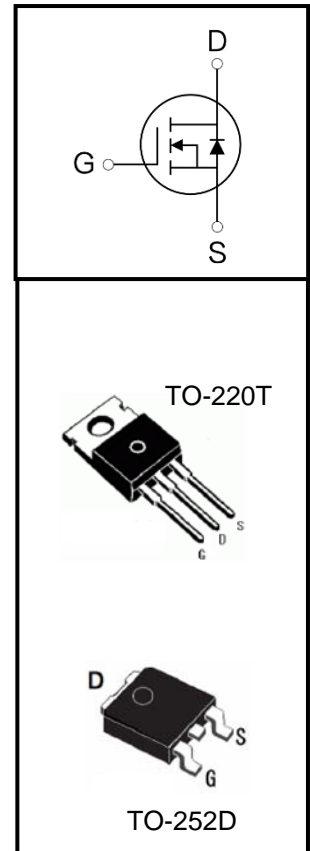
FEATURES

- Super Low Gate Charge
- 100% EAS Guaranteed
- RoHS compliant
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology



APPLICATIONS

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification



Device Marking and Package Information		
Device	Package	Marking
SR120N10D	T0-252-2L	SR120N10D
SR120N10T	T0-220-3L	SR120N10T

Absolute Maximum Ratings at $T_j = 25^\circ\text{C}$ unless otherwise noted			
Parameter	Symbol	Value	Unit
Drain-Source Voltage ($V_{GS} = 0\text{V}$)	V_{DSS}	100	V
Continuous Drain Current $T_C = 25^\circ\text{C}$ (note1)	I_D	50	A
Continuous Drain Current $T_C = 100^\circ\text{C}$ (note1)		30	A
Pulsed Drain Current (note2)	I_{DM}	150	A
Gate Source Voltage	V_{GSS}	± 20	V
Single Pulse Avalanche Energy (note3)	E_{AS}	240	mJ
Power Dissipation $T_C = 25^\circ\text{C}$ (note4)	P_D	70	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	$-55 \sim +150$	$^\circ\text{C}$

Thermal Characteristics			
Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (note1)	$R_{\theta JC}$	2.08	$^\circ\text{C/W}$

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise specified						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100V, V_{GS} = 0V, T_J = 25^\circ\text{C}$	--	--	1	μA
		$V_{DS} = 100V, V_{GS} = 0V, T_J = 55^\circ\text{C}$	--	--	5	μA
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20V$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.2	1.7	2.2	V
Drain-Source On-Resistance (note2)	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$	--	12	15	$m\Omega$
		$V_{GS} = 4.5V, I_D = 15A$	--	14	17	$m\Omega$
Dynamic						
Input Capacitance	C_{iss}	$V_{GS}=0V,$ $V_{bs}=50V,$ Frequency=1.0MHz	--	1200	--	pF
Output Capacitance	C_{oss}		--	180	--	
Reverse Transfer Capacitance	C_{rss}		--	4.7	--	
Gate Resistance	R_g	$V_{GS} = 0V, f = 1.0\text{MHz}$	--	2.0	--	Ω
Total Gate Charge	Q_g	VDD=50V ID=10A $V_{GS} = 10V$	--	23	--	nC
Gate-Source Charge	Q_{gs}		--	5.9	--	
Gate-Drain Charge	Q_{gd}		--	5	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DS} = 50V, I_D = 10A$ $V_{GS} = 10V, R_G = 10\Omega$	--	9.2	--	ns
Turn-on Rise Time	t_r		--	33	--	
Turn-off Delay Time	$t_{d(off)}$		--	40	--	
Turn-off Fall Time	t_f		--	48	--	
Body Diode Characteristics						
Continuous Body Diode Current	I_S		--	--	50	A
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{SD} = 20A, V_{GS} = 0V$	--	0.94	1.4	V
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}$ IS=10A $di_f/dt = 100A/\mu s$	--	48	--	ns
Reverse Recovery Charge	Q_{rr}		--	55	--	nC

Notes

1. The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
2. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. Limited by T_{Jmax} , starting $T_J=25^\circ\text{C}$, $L = 10mH$, $V_{DD} = 25V$, $V_{GS} = 10V$.
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Fig.1 Typical Output Characteristics

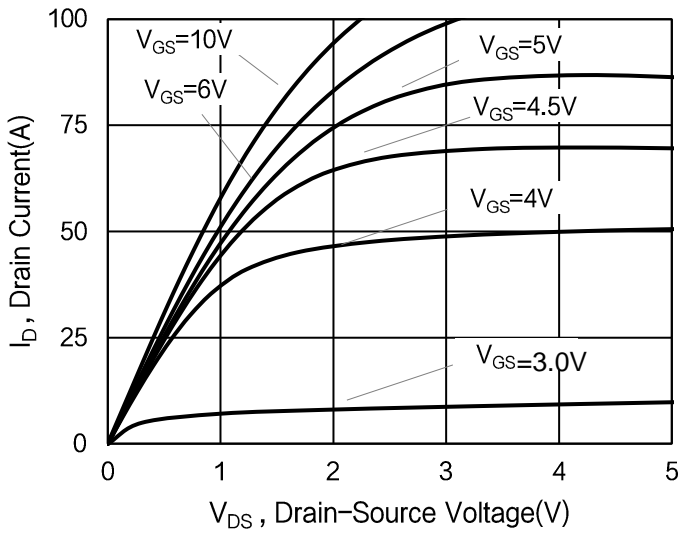


Fig.2 On-Resistance vs. G-S Voltage

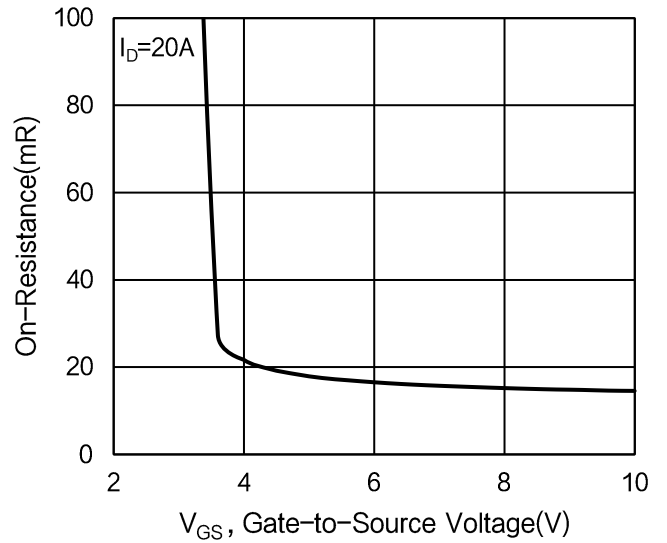


Fig.3 Forward Characteristics of Reverse Diode

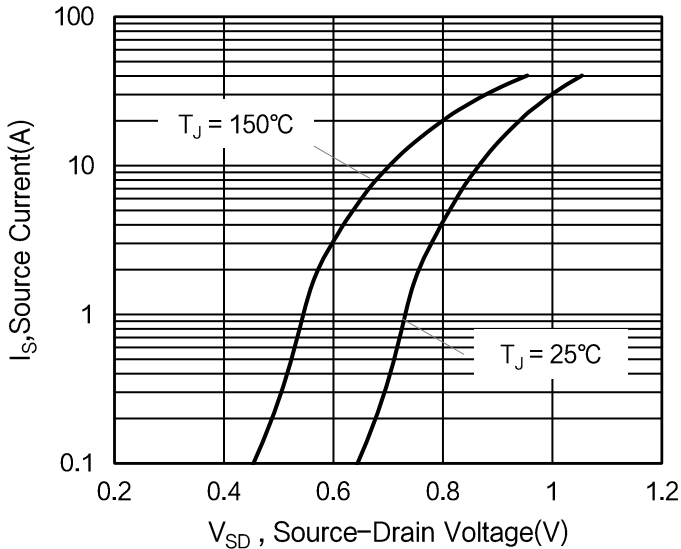


Fig.4 Gate-Charge Characteristics

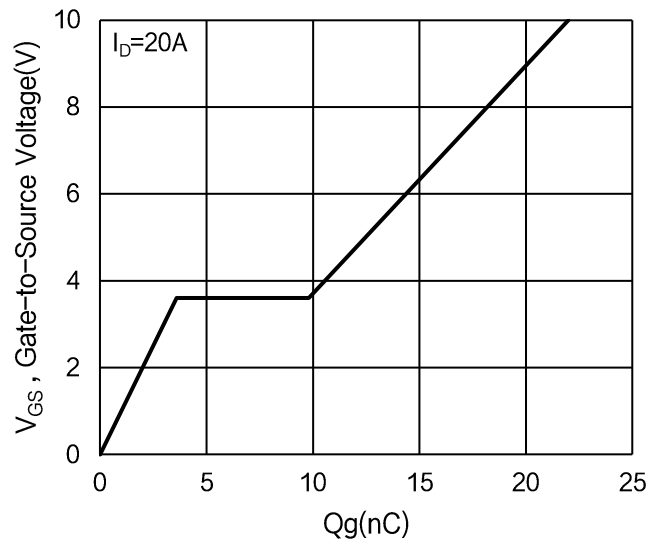


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

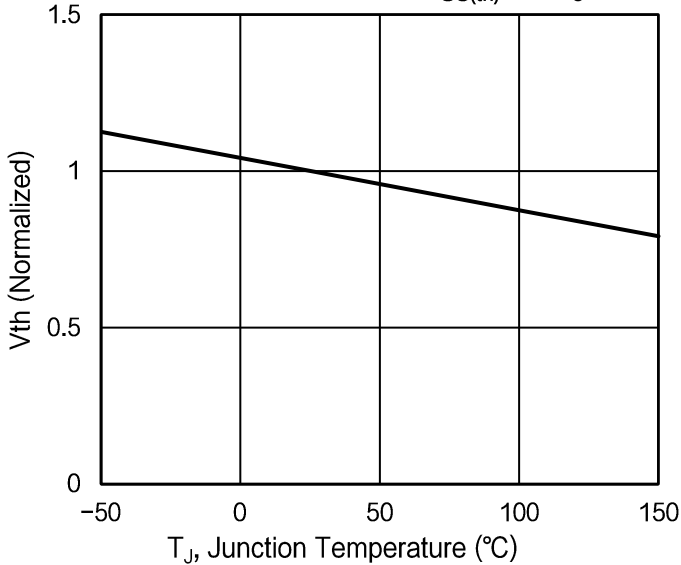
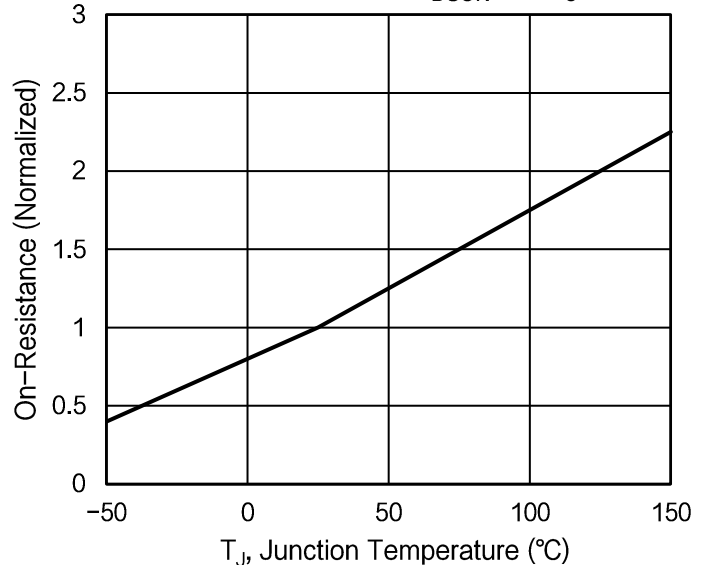


Fig.6 Normalized $R_{DS(on)}$ v.s T_J



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Fig.7 Capacitance

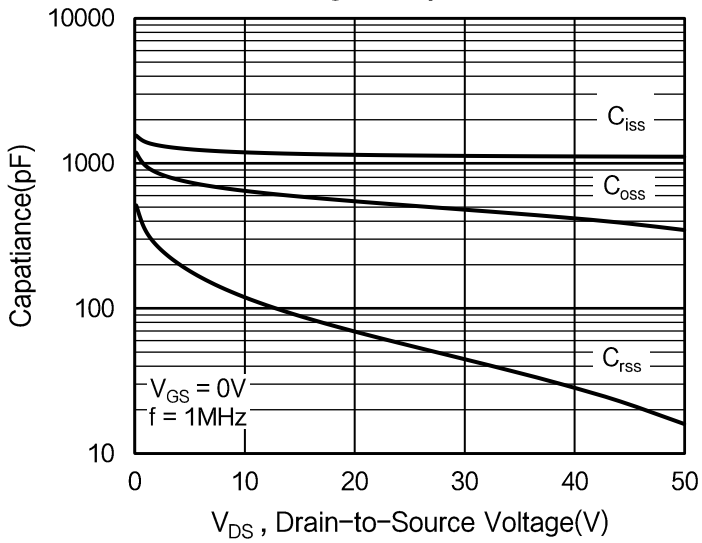


Fig.8 Safe Operating Area

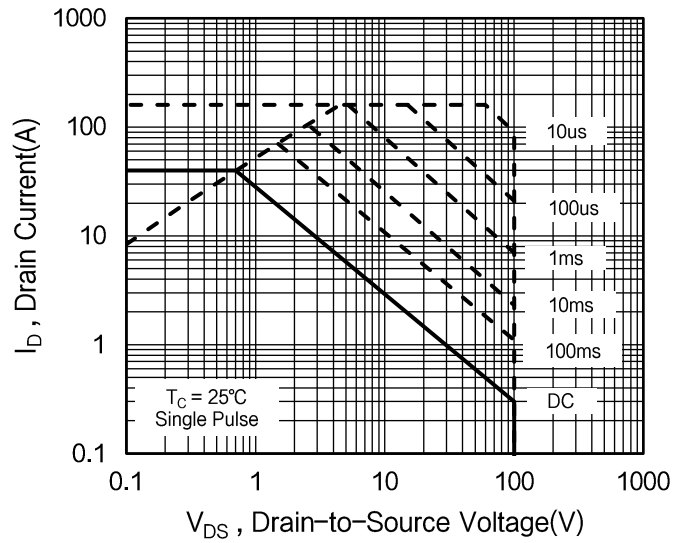


Fig.9 Normalized Maximum Transient Thermal Impedance

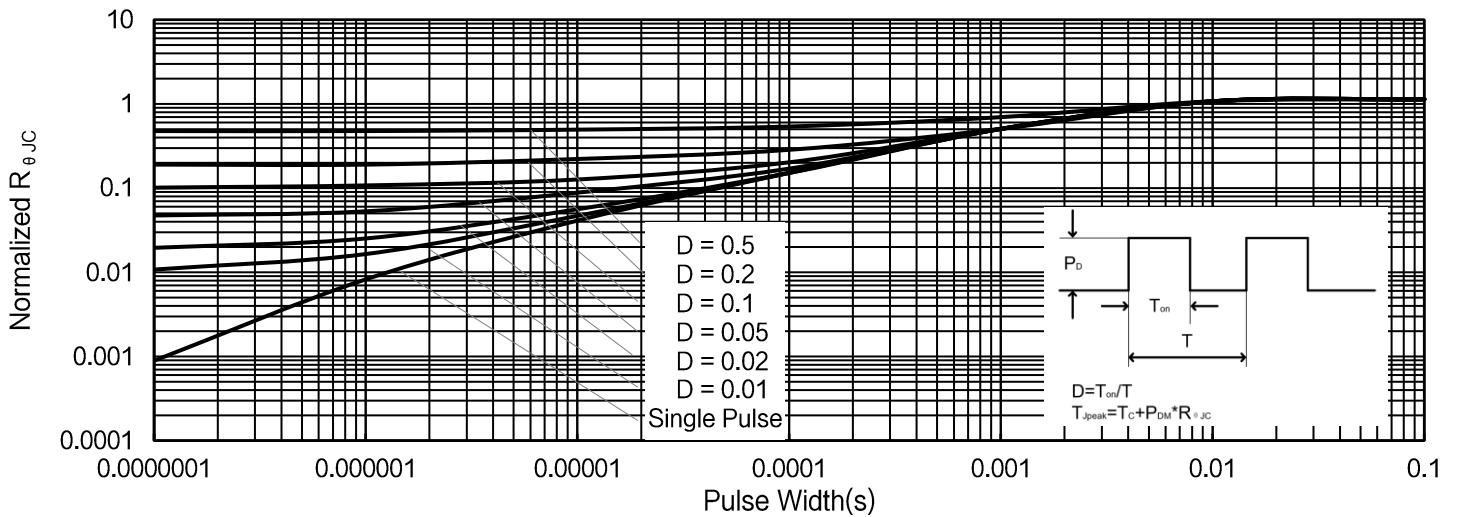


Figure A: Gate Charge Test Circuit and Waveform

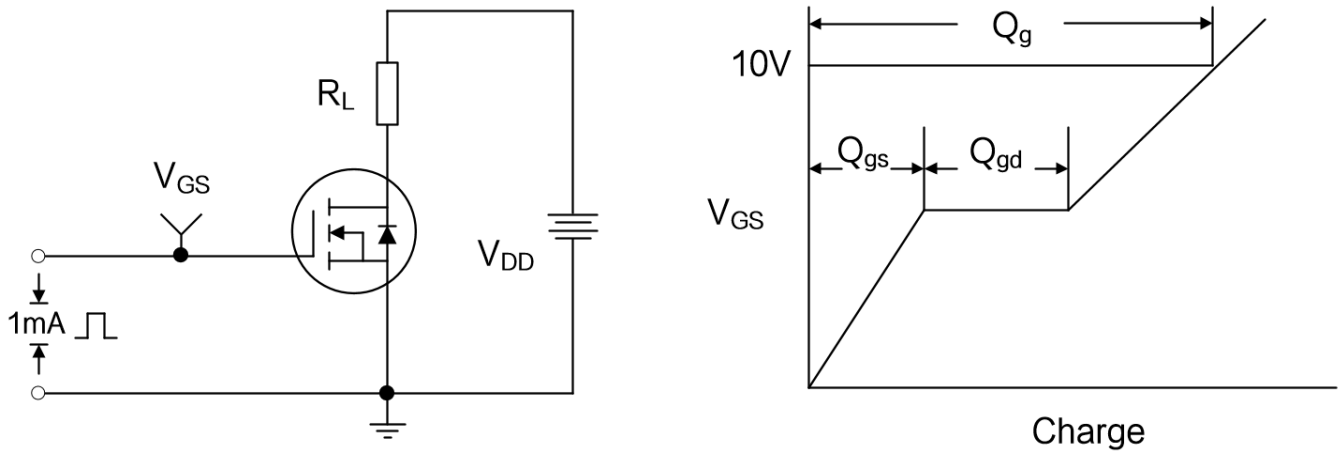


Figure B: Resistive Switching Test Circuit and Waveform

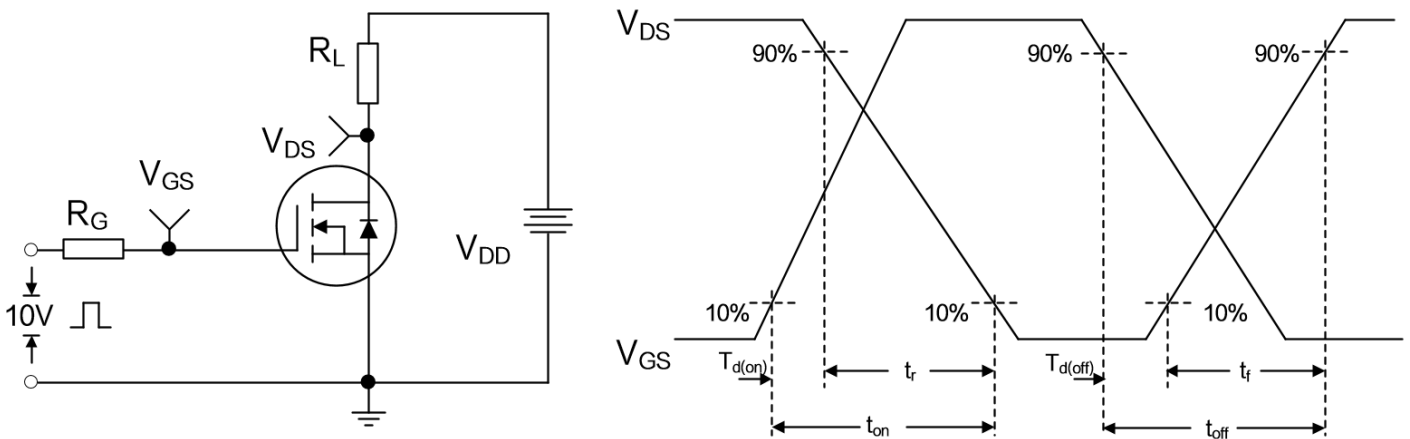
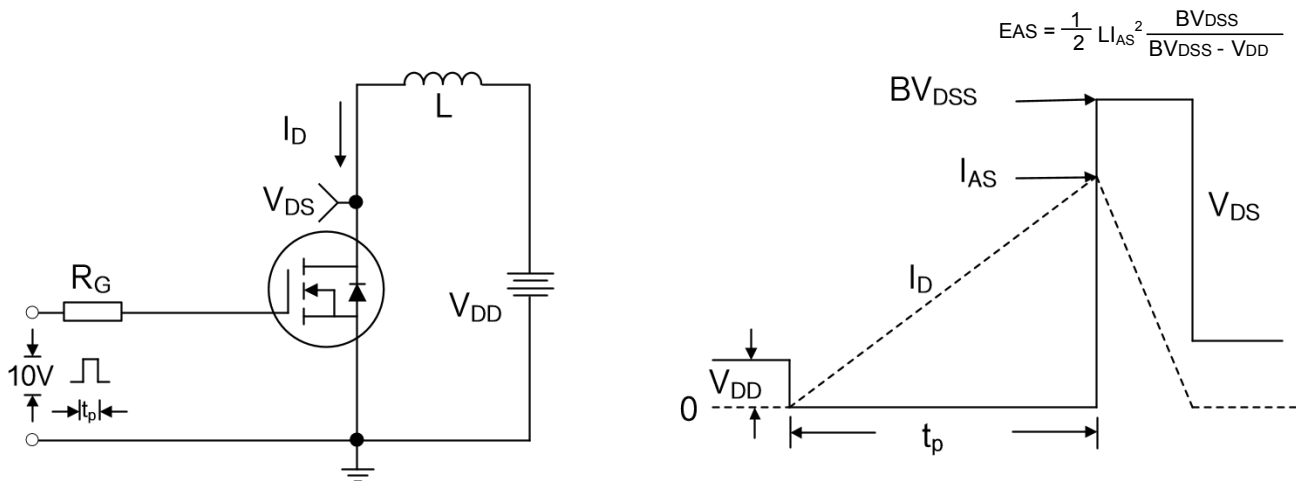
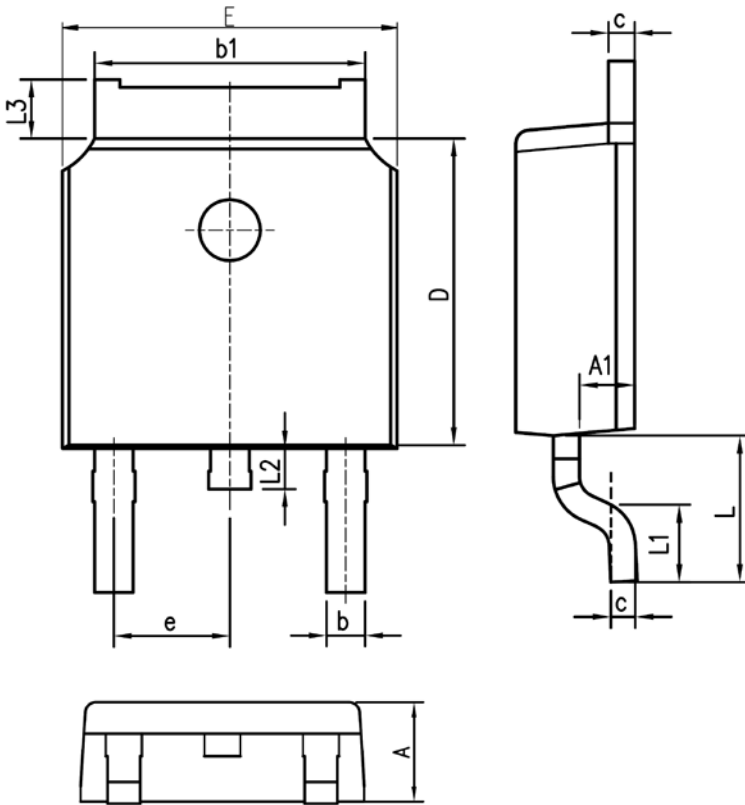


Figure C: Unclamped Inductive Switching Test Circuit and Waveform



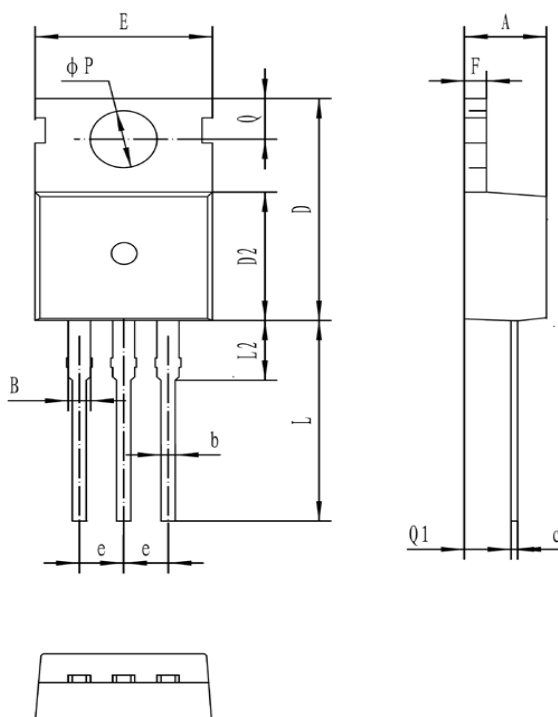
PACKAGE MECHANICAL DATA

DPAK TO-252

Unit: mm


SYMBOL	mm	
	MIN	MAX
A	2.10	2.50
A1	0.97	1.17
b	0.63	0.93
b1	5.13	5.53
c	0.40	0.60
D	5.80	6.40
E	6.30	6.90
e	2.286BSC	
L	2.50	3.30
L1	1.20	1.80
L2	0.60	1.00
L3	0.85	1.30

TO-220T



符号 symbol	MIN	MAX
A	4.30	4.70
B	1.10	1.40
b	0.70	0.95
c	0.40	0.65
D	15.20	16.20
D2	9.00	9.40
E	9.70	10.10
e	2.39	2.69
F	1.25	1.40
L	12.60	13.60
L2	2.80	3.20
Q	2.60	3.00
Q1	2.20	2.60
P	3.50	3.80

产品名称： SR120N10D/T

文档类型：说明书

版 权：意盛微（上海）电子有限公司

公司主页：WWW.SXCAI.COM

版 本： 1.0

修改记录：

1. 原本
